Request for Proposal

Procurement of Services for the Establishment of Semiconductor Education & Research Clusters (SERCs) under the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I

A(01)/PSEB/2025/29

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Contents

1. **Introduction to PSEB**

Pakistan Software Export Board (PSEB) is an entity under the Ministry of IT & Telecom mandated to act as One Stop Shop on behalf of Government of Pakistan and ensuring of sustainable growth, development of the industry and enhancing of IT & ITeS exports. One of the objectives of PSEB is availability of skilled resource equipped with latest technologies for the IT Industry. In order to help increase the employability and to fill the supply gap for industry-ready skilled resource, PSEB under the guidance of Ministry of IT and consultation with IT Industry is initiating a series of HR development program, one of the said programs is equipping of the IT professionals and ICT & Non-ICT graduates with latest technologies by the ICT Industry Professionals which will help in enhancing the number and quality of HR workforce available to Pakistan IT & ITeS industry

2. **Introduction to the Project**

The National Semiconductor Human Resource Development Project (NSHRDP) is a strategic initiative aimed at establishing Pakistan as a competitive hub for semiconductor design talent. Central to this initiative is the creation of Semiconductor Education & Research Clusters (SERCs) in three key regions SERC-North, SERC-Centre and SERC-South by leveraging and strengthening the capabilities of leading public sector universities. These clusters will focus on formal undergraduate and postgraduate education, curriculum modernization, and infrastructure development to produce over 2,200 highly skilled engineers by 2029. The project also aims to promote indigenous chip design R&D and enhance employability by aligning academic outcomes with global industry standards.

This procurement directly supports overall objective of the project, including:

- **Component I: Semiconductor Education & Research Clusters (SERCs)**: Focused on formal academic training, this component aims to strengthen undergraduate (BS/BE) and postgraduate (MS/PhD) programs in electronics, electrical engineering, and computer engineering disciplines, through access to state-of-the-art Electronic Design Automation (EDA) tools and compute infrastructure.
- **Component II: Upskilling Training Programs (USTPs):** Targeting professionals and industry practitioners, this component seeks to deliver fast-track, modular training in digital and analog chip design, verification, layout, and embedded systems, aligned with real-world industrial demands.

- **Component III: Centralized Electronic Design Automation (EDA) Tools:** This component plays a critical enabling role by providing shared access to industry-standard EDA software, silicon IP repositories, and remote design environments through a centralized cloud-based infrastructure. This component ensures that both SERCs and USTPs have the necessary digital tools and support to deliver high-quality semiconductor education and training.

3. Objectives of Procurement

The overarching objective of this procurement is to establish and operationalize three region-wise distributed Semiconductor Education & Research Clusters (SERCs)—namely SERC-North, SERC-Centre and SERC-South, as flagship academic and research hubs for developing a national talent pipeline in semiconductor design and related domains. These clusters will be established within selected public sector universities through a competitive selection process and will be supported to build institutional capacity, modernize curriculum, and facilitate industry-aligned research and development in the fabless semiconductor ecosystem.

Specifically, the procurement aims to achieve the following objectives:

3.1. Establish Regional Clusters of Academic Excellence

Create dedicated semiconductor education clusters within leading public universities across three major regions of Pakistan SERC-North, SERC-Centre and SERC-South. These clusters will serve as focal points for formal degree-based education and research in semiconductor technologies, enabling a consistent supply of trained engineers and researchers.

3.2. Curriculum Revamp and Integration of Semiconductor Design

Support universities in the modernization of undergraduate and postgraduate curricula in Electrical, Electronics, Computer Engineering programs and any other disciplines as approved by the PSC (Project Steering Committee). The objective is to embed IC design-focused content— such as Digital Logic Design, Digital IC Design, Physical Design, Analog/Mixed Signal Design, and Verification—into formal coursework to align with evolving global and local industry demands.

3.3. Promote Indigenous R&D in Chip Design

Foster innovation and research among postgraduate students and faculty by facilitating collaborative research projects in areas of national and strategic relevance. Strengthen linkages with public and private local and international R&D organizations to ensure that the clusters contribute not only to workforce development but also to the creation of IP and innovation in chip design and verification.

3.4. Enable Collaboration with Industry for Employability

Ensure close collaboration with semiconductor companies, design houses, and technology startups operating in Pakistan and abroad to align training and academic programs with market requirements. Enable joint curriculum development, industry seminars, internships, and project supervision to ensure that graduating students are industry-ready and employable.

3.5. Contribute to National Semiconductor Strategy

Support the broader National Semiconductor HR Development Program (NSHRDP) and the Government of Pakistan's ambition to position the country as a competitive destination for chip design and high-tech R&D. The establishment of SERCs will build the academic backbone required for a sustainable fabless semiconductor ecosystem in Pakistan till 2030.

3.6. Deliver Measurable Human Resource Development Outcomes

Train approximately 1,000 engineers by 2030 under SERC Phase-I through formal undergraduate and postgraduate degree pathways. Graduates should be trained across high-demand sub-domains including Digital IC Design, Verification, Analog and Mixed Signal Design, and RF IC Design, with clear monitoring and evaluation frameworks to track progress and placement outcomes.

3.7. Training Delivery Model

The three SERC-regions will constitute three lots as follows to execute the program:

    a. Lot-I: SERC-Southern (Sindh & Baluchistan)
    b. Lot-II: SERC-Central (Punjab)
    c. Lot-III: SERC-Northern (ICT, KP, AJK & GB)

Approximately, 1,000 trained engineers will be developed in the three (03) SERCs by 2030, across undergraduate and postgraduate levels in semiconductor design and verification under SERC Phase-I.

The public sector universities will in their respective SERC-Regions based on the location of their Principal Seat.

4. Scope of Work

The selected universities will be responsible for the establishment, execution, and scaling of Semiconductor Education & Research Clusters (SERCs) in designated regions SERC-North, SERC-Centre and SERC-South of Pakistan. Each SERC will function as a regional hub to train undergraduate and graduate students in semiconductor design disciplines, facilitate research and development, and actively engage with the domestic semiconductor industry. The scope of work includes but is not limited to the following activities:

4.1. Cluster Establishment & Operationalization

- Establish and manage SERCs as per regions allocated (North, Centre & South).
- Coordinate with the Project Implementation Unit (PIU) for phased rollout across approximately nine universities.
- Form intra-university and inter-university coordination mechanisms within clusters.

4.2. Curriculum Development & Academic Integration

- Review and revise existing undergraduate and graduate programs (e.g., BS/BE in EE/CE/CS, MS in relevant specializations) to align with industry needs in consultation with the TAC (Technical & Advisory Committee) and subsequent approval of PSC (Project Steering Committee).
- Integrate advanced modules on Digital IC Design, Verification, Analog/Mixed-Signal Design, and EDA tools.
- Ensure curriculum incorporates practical project-based learning and exposure to commercial workflows.
- Strengthen linkages with public and private local and international R&D organizations to ensure that the clusters contribute not only to workforce development but also to the creation of IP and innovation in chip design and verification.

4.3. Training & HR Development

- Produce approximately 1,000 trained engineers by 2030 under Phase-I RFP, with domain-specific distribution:
    - ~70% at undergraduate level
    - ~30% at graduate level
    - ~50-60% in Digital Design & Verification
    - ~30-40% in Digital Integrated Chip Design
    - ~10% in other emerging areas (RF, Analog, Mixed Signal, etc.)
- Conduct regular workshops, and project-based training within academic calendars.
- Monitor and report training progress and outcomes per cohort.
- Based on funds availability of funds, executing agency may change the target number of trained engineers.

4.4. Lab & Infrastructure Setup

- The provision of well-equipped Labs and Classrooms will primarily be the responsibility of the selected universities and will be the part of evaluation process. However, the project will take care of upgradation of the lab infrastructure as per the needs and availability of funds. This upgradation may include provision of high-end servers & workstations, UPS, FPGA Kits, Multimedia projector, and networking equipment for Labs.
- Having required Electronic Design Automation (EDA) and other tools will be a plus point however, access to a centralized EDA tools repository will be provided under this project.

4.5. Industry Linkages & Research Promotion

- Facilitate partnerships with local and international chip design companies, R&D labs, and incubators.
- Promote indigenous chip design research relevant to commercial and defense applications.
- Encourage collaborative R&D through graduate thesis projects, industry-sponsored research, or joint development programs.

4.6. Monitoring, Reporting & Quality Assurance

- Regularly submit reports on training enrollment, completion rates, lab usage, and HR deployment.
- Maintain quality standards through internal and third-party assessments.
- Coordinate with PIU to conduct evaluations and make continuous improvements.

4.7. Graduate Employability & Placement Facilitation

- Develop graduate placement strategies. A complete detail existing mechanism, policies and responsible entity within the university shall be submitted with proposal.
- Embed employability KPIs within academic and training structures.
- Maintain graduate follow-up records to support impact assessment and alumni tracking.

4.8. Knowledge Dissemination & Outreach

- Provide a special section to promote SERC activities on university portal.
- Organize seminars, webinars, student competitions, and public engagement activities.
- Create content (case studies, toolkits, presentations) to share learning and success stories across the ecosystem.
- Host annual cluster reviews or industry-academia symposiums.

4.9. Sustainability Planning

- Design a sustainability model for each SERC beyond project completion.
- Explore opportunities for public-private partnerships, paid industry programs, and government support to continue operations.

5. Target Outcomes

The Semiconductor Education & Research Clusters (SERCs) aim to serve as the cornerstone of Pakistan's long-term strategy to build a globally competitive semiconductor workforce. This initiative is designed not only to meet the current industry demand but also to position Pakistan as a viable player in the global semiconductor value chain over the next decade. The key outcomes targeted under this component are outlined below:

5.1. Human Resource Development (HRD)

Approximately, 1,000 trained engineers will be developed by 2030 across undergraduate and postgraduate levels in semiconductor design and verification under SERC Phase-I.

- BS/BE Level: ~7,00 engineers
- MS Level: ~300 engineers
- Training will be aligned with international benchmarks in VLSI, Digital/Analog Design, and Verification.

- At least 60% of the HR trained is expected to find direct placement in local or international semiconductor companies within 6 months of graduation.
- Develop a scalable talent production pipeline that can be expanded post-2029 to support continued growth.

5.2. Cluster-Based Academic Integration

In each region, the selected university will ensure strong linking with other universities and relevant institutions to:

- Share curriculum, infrastructure, and faculty development programs.
- Integrate IC design tracks in existing BS and MS programs.
- Build localized ecosystems tailored to each region's industry needs.

5.3. Revamped Academic Curriculum

- Revise and modernize semiconductor-related courses in EE, Electronics, CE, and CS disciplines at both undergraduate and graduate levels.
- Incorporate industry feedback through regular engagement with PIU.
- Embed hands-on lab training with academic Electronic Design Automation (EDA) tools into academic semesters.

5.4. Indigenous Research and Design Capabilities

- Strengthen applied R&D by involving postgraduate students in industry-relevant projects in Digital, Mixed-Signal, and Analog/RF IC Design.
- Enable tape-out readiness by ensuring students graduate with at least one complete design cycle experience.

5.5. Industry Engagement and Employment Enablement

- Establish a collaborative framework with local and international companies to ensure curriculum and project relevance.
- Incorporate internship programs and joint supervision of capstone projects with industry experts.
- Develop career placement pathways through career fairs, MoUs with companies, and project-based evaluation.

5.6. Capacity Building of Institutions

- Upgrade labs with industry-grade EDA tools and servers through PIU.
- Train faculty members to international competency standards.
- Build institutional capabilities for continuous program delivery post-project life.

5.7. Promote Diversity and Inclusion

- Ensure geographical and gender diversity in enrollment across the clusters.
- Target at least 20% participation from underrepresented areas and women in engineering programs.

5.8. Long-Term National Impact

- Lay the foundation for a fabless chip design ecosystem in Pakistan.
- Contribute to reducing reliance on foreign engineering talent by creating home-grown capabilities.
- Serve as a model for future high-tech talent development projects across other domains like AI, quantum computing, and telecom.

6. Eligibility Criteria

To ensure the successful implementation and sustainability of the Semiconductor Education & Research Clusters (SERCs), applicants must meet the following eligibility criteria. These criteria are designed to assess the institutional capacity, technical competence, infrastructure readiness, and alignment with national objectives for semiconductor talent development. (TAC is requested to provide detailed criteria)

6.1. Type of Eligible Institutions

Bidding public sector universities must be one of the following:

- HEC-recognized public universities offering undergraduate and postgraduate degree programs in Electrical Engineering (EE), Computer Engineering (CE), Electronics Engineering, Mechatronics Engineering, or Computer Science or any other discipline subject to approval of Project Steering Committee.
- Research institutes involved in semiconductor, microelectronics, or IC design.
- Active liaising (preferably contracts/MoUs) with multiple academic and R&D institutions (public/private), for R&D in the field of Semiconductor Technologies.
- Have valid accreditation from relevant bodies such as PEC & HEC
- Have at least 40 for MS and 50 for UG seats approved from respective authorities like PEC & HEC.

6.2. Academic and Programmatic Readiness

- Have ongoing undergraduate (BE/BS) or graduate (MS/PhD) programs in the relevant disciplines.
- Demonstrate faculty strength with expertise in Digital IC Design, Design Verification, Analog/Mixed Signal Design, RF IC, VLSI, etc.
- Show evidence of curriculum alignment or readiness to revise existing curriculum to integrate semiconductor education tracks.

6.3. Project and Institutional Experience

- Proven track record of research, training, or curriculum development in IC design, microelectronics, or embedded systems.
- Evidence of industry collaboration, MoUs, or participation in funded technical training or R&D projects.
- Experience in implementing government or donor-funded programs will be an added advantage.

6.4. Human Resource Capacity

- Must have a minimum number of full-time faculty in relevant domains verified through relevant experience in semiconductor technologies like tape-out, transcripts, etc. (e.g., 5+ for BS programs, 4 or more for MS programs - as total number of consortium partners).
- Institutions must nominate a dedicated Project Lead (preferably PhD with relevant expertise) for coordination with the PIU.
- Must have the administrative and technical support staff to ensure smooth implementation.

6.5. Institutional Commitment

- Commitment to deliver project outcomes as per timelines and quality benchmarks.
- Willingness to provide in-kind support where needed (e.g., lab space, utilities, non-project-funded personnel).
- Must agree to monitoring, evaluation, and reporting mechanisms as defined by the PIU.

6.6. Legal and Financial Compliance

- Must be a registered legal entity in Pakistan with the ability to receive and manage project funds.
- Must have auditable financial records and a designated finance office/department.
- Must be in good standing with HEC and relevant regulatory bodies (e.g., PEC).

6.7. Gender and Geographic Diversity

- Bidding public sector universities should demonstrate a commitment to inclusivity, including the promotion of female participation and outreach to underserved regions.
- Preference may be given to bidding public sector universities in provinces or regions underrepresented in the high-tech sector, to ensure balanced national development.

The bidding public sector universities from 3 regions SERC-North, SERC-Centre and SERC-South are encouraged to apply.

- The bidding public sector universities may partner with International Trainings/Chip Design Firms/companies and regional centers to extend outreach. Partnerships with

International training/chip design firms/companies will be considered an added value addition.

7. Proposal Requirements

All bidding public sector universities are required to submit a complete proposal package comprising a Technical Proposal and a Financial Proposal separately following single stage two envelope process of PPRA. The proposals must be clearly labeled and submitted by the deadline mentioned in the RFP. Incomplete proposals or those not meeting the format requirements will be rejected.

7.1. Technical Proposal

The Technical Proposal must demonstrate the applicant's understanding of the program, their technical capacity to deliver the training, and a clear roadmap for execution and outcomes. It should include the following sections:

7.1.1. Institutional Profile

- Overview of the applying institute
- Legal status and relevant registrations (HEC, SECP, etc.)
- Vision, mission, and relevance to semiconductor education
- Key personnel and their qualifications

7.1.2. Relevant Experience

The bidding public sector universities must demonstrate proven experience and institutional capacity in semiconductor education, training, and research. The proposal should include:

- Summary of Past Experience: A clear account of prior activities in delivering undergraduate/graduate-level education, specialized training programs, or upskilling initiatives in areas such as Digital IC Design, Verification, Analog/Mixed-Signal Design, and Embedded Systems.
- R&D and Innovation Projects: Evidence of successfully executed research projects, patents, or funded initiatives (national or international) relevant to semiconductor design, VLSI, microelectronics, or chip-related domains.
- Industry Collaborations: Documentation of partnerships with local or international semiconductor companies, design houses, or technology firms, especially those involving internships, joint research, tool access, or workforce development.
- Academic Initiatives: Participation in or establishment of centers/labs such as EDA labs, microelectronics research centers, or chip design programs at university/cluster level.

- Training/Project Summaries: At least two (2) examples of relevant training programs, workshops, or research projects delivered in the past, including details on:
    o Duration, scope, and curriculum focus
    o Number of participants trained or beneficiaries impacted
    o Tools/technologies used (EDA, verification, IC design platforms, etc.)
    o Documented outcomes (e.g., student employment, project completions, publications, prototypes, or chip tape-outs)

Preference will be given to bidding public sector universities that demonstrate a proven track record of at least two (02) years of successful HR development, measurable outcomes, and strong linkages with industry and global academia.

7.1.3. Curriculum and Academic Plan

- Strategy for curriculum alignment with industry-standard semiconductor domains: Digital IC Design, Analog/Mixed Signal, Design Verification, etc.
- Integration of hands-on training using academic EDA tools.

7.1.4. Faculty and Human Resource Plan

- List of trainers, faculty, and technical staff (with CVs in annexures).
- Plan to strengthen human resources through training-of-trainers (ToT) or partnerships.

7.1.5. Lab Infrastructure Plan

- Current lab infrastructure, hardware/software tools available.
- Gaps identified and proposed upgrades (if any).
- Plan for sharing/accessing centralized resources (if applicable).

7.1.6. Student Engagement & Selection Plan

- Criteria and process for student selection (at BS and MS levels).
- Plan for student mentorship, project assignments, and evaluation.
- Strategy to ensure diversity, inclusivity, and geographic balance.

7.1.7. Industry Linkages & Employability

- Existing industry collaborations or MoUs (with documentation).
- Plan for industry advisory support, internship opportunities, and placement pathways.
- Mechanism to align student projects with real-world design challenges.

7.2. Financial Proposal

The Financial Proposal must present a transparent, detailed, and justifiable budget for the proposed training programs. It should include:

7.2.1. Batch-wise Cost Summary

- Cost estimates based on proposed batch size
- Multiple batch scenarios (if applicable)

7.2.2. Payment Milestones

Semester fee and student stipend will be paid under this program. The participating bidding public sector universities are to provide the students fee structure and fee receipt schedule. A formal agreement will be signed with the Project Awardee to comprehensively cover the payment terms and conditions.

7.3. Mandatory Attachments

The following documents must be included in the proposal package:

Sr. #	Required Document
1	University Profile
2	Relevant Academic Programs
3	Faculty Details
4	Institutional Capacity & Infrastructure
5	R&D and Industry Linkages
6	Evidence of prior training programs/workshops in IC design.
7	Placement support details
8	Any international collaborations

The following documented details shall be made available in the technical proposal:

7.3.1. Legal Registration and Operational Status
The bidding public sector universities must be legally registered with the relevant authorities in Pakistan providing appropriate documentations.

7.3.2. Relevant Institutional Capacity and Experience

- Proven track record of delivering technical education or training programs, particularly in fields such as:
    - Electrical/Computer Engineering
    - Embedded Systems

- o Digital Design, RTL, SoC Development
- o Microelectronics / Semiconductor Engineering
- The bidding public sector universities must have conducted at least two (2) IC design, electronics, or embedded systems-related training programs in the last five (5) years, or demonstrated equivalent R&D project experience.
- Organizations should attach:
  - o Project summary reports
  - o Completion certificates
  - o Feedback/evaluation results (if available)

7.3.3. Qualified Faculty and Technical Staff

- Availability of full-time or part-time trainers with industry or academic experience in semiconductor chip design or relevant domains.
- Trainers should ideally have expertise in tools like Cadence, Synopsys, Mentor Graphics, Verilog/SystemVerilog, SPICE, etc.
- At least two instructors per batch must have 5+ years of teaching or IC industry experience.
- CVs including complete details of the trainers, lab assistants, etc.

7.3.4. Infrastructure and Tool Access

- The bidding public sector universities will be provided a limited lab upgradation facility as mentioned under cluase#4.4, however, the participating universities are required to provide following details to assess their existing experience in semiconductor education and R&D:
  - Lab space with computing resources.
  - Internet connectivity
  - Available EDA tools
- The bidding public sector universities that do not have currently industry standard tool licenses must show their ability to acquire them (via service agreements, university licensing, or partnerships) before the commencement of the trainings, if declared the Most Advantageous bidding public sector universities.
- A lab infrastructure summary and photos or virtual tour.

7.3.5. Industry Collaboration / Placement Support

- Active industry collaboration is mandatory.
- At least two letters of support or MoUs must be provided from IC chip design companies, semiconductor startups, or relevant tech firms.

7.3.6. Monitoring, Assessment & Data Reporting Capacity

- The bidding public sector universities must commit to:
  - Maintaining attendance records
  - Conducting pre/post assessments

- Tracking employment outcomes
- Submitting timely reports to PIU
- Demonstrated use of a Learning Management System (LMS), MIS, or internal data systems will be an advantage.

7.3.7. Financial and Administrative Capacity

- The bidding public sector universities must have the ability to manage public funding transparently and comply with procurement, financial, and audit requirements. Submit:
  - Last two years of audited financial statements
  - Contact information of finance manager

7.3.8. Compliance with Government and Program Policies

- Bidding public sector universities must not be blacklisted by any government agency or donor organization.
- They must agree to comply with all terms, deliverables, and quality assurance mechanisms defined by the PIU and/or funding agency.

8. Evaluation Criteria

All submitted proposals will undergo a two-step evaluation process—technical and financial—carried out by a designated Evaluation Committees.

Only those proposals that meet the eligibility criteria outlined in Section 6 and are deemed technically responsive (achieving the minimum qualifying score of 70% in the technical evaluation) will proceed to the financial evaluation stage.

The following weighted evaluation criteria will be used to assess and rank the proposals:

8.1. Technical Evaluation (Total Weight: 70%)

Proposals will be scored based on the following technical criteria:

Sr. #	Evaluation Area	Weight (%)	Scoring Basis
1.	**Curriculum Development & Academic Relevance**	25%	Alignment of revised BS/MS curricula with NSHRDP objectives; integration of semiconductor core courses (Digital Design, Verification, Analog/Mixed Signal, etc.); incorporation of hands-on labs and

			academic EDA tools; academic-industry alignment. (Sr#4)
2.	**Faculty Expertise & Research Profile**	**20%**	Qualifications and research background of faculty/trainers in IC design, verification, and related domains; publications, patents, prior semiconductor training/research programs, and ability to supervise UG/PG projects.
3.	**Institutional Capacity & Infrastructure Readiness**	**15%**	Availability and readiness of labs, computing resources, EDA licenses, and support staff; demonstrated ability to host 100+ students per year across programs; integration with Learning Management Systems (LMS).
4.	**Industry Linkages & Employability Pathways**	**15%**	MoUs/partnerships with semiconductor companies, defense R&D, and global design houses; internships, job placement pathways, and industry co-supervised projects for students.
5.	**Research & Innovation Contributions**	**10%**	Capability to promote indigenous chip design R&D; track record in collaborative research, IP creation, and ongoing or past funded projects.
6.	**Project Management & Governance Approach**	**5%**	Mechanisms for academic monitoring, curriculum review boards, student performance tracking, reporting, and committee oversight.
7.	**Scalability & Sustainability Plan**	**10%**	Long-term institutional commitment to sustaining semiconductor programs beyond project funding; future student intake plans, self-sustainability measures, and regional/national outreach.

Note: Minimum **70% qualifying marks** will be required in the technical evaluation to qualify for second stage of financial proposal evaluation.

8.2. Financial Evaluation (Total Marks: 30)

The selected/qualified SERCs will be funded through this project for delivery of train the students of discipline as mentioned under para no. 4.2 enrolled under undergraduate (7th & 8th Semesters) and postgraduate (02 years study program as approved by the HEC) programs in semiconductor technologies.

The selected SERCs member universities will also be reimbursed certain amount of institutional overheads like planning, coordination, TA/DA for project related activities.

The universities participating in the NSHRDP are required to submit following details under Financial Proposal, including but not limited to:

a. Current number of students enrolled in the disciplines mentioned under clause#4.2.
b. Student selection criteria for enrolled students.
c. Curriculum being taught to the students under discussion, specifically mention the number of courses being taught during the length of trainings as mentioned below:
   i. Undergraduates: 7th & 8th Semesters
   ii. Postgraduates: 02 years MS degree program (~ 04 semesters) as approved by the HEC and/or PEC.
d. Fee structure being charged to the students under discussion.
e. Teaching Allowance for permanent Faculty Members engaged in teaching specialized technological courses.
f. Current Remuneration Package for the Teaching Visiting Faculty (TVF) or Industry Trainers.

The evaluation of Financial Proposals will be based on the following criteria:

#	Criterion	What evaluators compare	Max marks	Simple scoring method
1	UG cost per student (annual)	Total PSEB-funded UG cost per student per academic year (tuition/fees claimed from project + teaching allowances claimed + pro-rated OPEX/ overhead attributable to UG)	7	Lowest gets full marks. Others: $(L_1 / L_i) \times 7$
2	MS cost per student (annual)	Total PSEB-funded MS cost per student per academic year (tuition/ fees claimed from project + teaching allowances claimed + pro-rated OPEX/ overhead attributable to MS)	7	Lowest gets full marks. Others: $(L_1 / L_i) \times 7$
3	Operating expenses & institutional overhead	OPEX + overhead as % of total evaluated financials (after removing fixed/capped items). Lower % = better value	6	Lowest % gets full marks. Others: (Lowest% / Bidder%) × 6

| 4 | Fee structure clarity & schedule | Transparency of fee heads, per-semester/annual schedule, receipt plan | 5 | 3 = complete, unambiguous, per schedule; 1–2 = minor gaps; 0 = missing/unclear |
| 5 | University cost-sharing / in-kind support | Monetized value of in-kind (labs, space, utilities, licenses, admin support) or fee waivers the university commits | 5 | Highest contribution gets full marks. Others:(Bidder / Highest) $\times$ 5 |

L_1: Lowest Offered Cost
L_i: Offered Cost

8.3. Mandatory Eligibility Criteria Checklist

Before the bidding public sector universities submit their Proposals, within the stipulated time mentioned in this Request for Proposal document, bidding public sector universities are required to make sure that following mandatory requirements of this RFP document are fulfilled. These requirements must be furnished at the time of submission of Proposal. Non-submission of any one of the following applicable requirements shall result in disqualification:

Sr#	Mandatory Eligibility Criteria Checklist (If compliant, please check, otherwise put a Cross in the Mark Column)	Mark (Yes/No)
1.	Proof of Certificate of Incorporation or Registration or equivalent with relevant authorities.	
2.	Proof of NTN Certificate	
3.	Proof of GST Certificate	
4.	Original affidavit (not older than one month) on Stamp Paper(s) of worth Rs.100 or more that the bidding public sector universities is an active tax payer and has submitted its tax return for the preceding fiscal year. **Tax payer list serial number (downloadable from FBR's website) is also to be mentioned.**	
5.	"**TECHNICAL PROPOSAL –** *Procurement of Services for the Establishment of Semiconductor Education & Research Clusters (SERCs) under the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I",* Technical Proposal must be submitted on E-Pads (https://eprocure.gov.pk/). Bidding public sector universities are to make sure that Financial Proposal is **not** part of the Technical Proposal in any form.	

| | "**FINANCIAL PROPOSAL -** *Procurement of Services for the Establishment of Semiconductor Education & Research Clusters (SERCs) under the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I",* Financial Proposal must be submitted on E-Pads (https://eprocure.gov.pk/). The Financial Proposal should not be part of Technical Proposal in any form. | |

Note: Bidding public sector universities <u>are required to submit</u> *filled, signed & stamped copy of the above checklist* along with the Proposal.

8.4. Other mandatory Instructions to bidding public sector universities

An undertaking, on the bidding university/entity's official letterhead, confirming compliance with the agreed deliverable timelines, effective from the date of issuance of the Purchase Order and/or execution of the Contract.

Based on justifiable reasons, the PSC (Project Steering Committee) may extend the timelines of deliverables.

8.5. Technical Evaluation Criteria

During the technical evaluation no amendments in the Proposals shall be permitted. Bidding public sector universities who obtain at least 70% marks in technical evaluation criteria will be declared technically qualified bidding public sector universities.

An evaluation committee appointed by the executing agency will evaluate Technical Proposals based on their compliance with the RFP and by applying the evaluation criteria and the point system, specified below:

Sr#	Description	Max. Score	Marks Allocation	
1	Bidding public sector universities Profile (Registered age)– **(Form B2)**	10	01 mark per year (Max. 10 Marks)	10
2	**Research and Innovation Contributions:** Experience of the Institutions. (Purchase Orders / Completion certificate and/or	30	Running UG & PG EE programs with semiconductor related courses for 3 or more years including research and innovation outcomes	30
			Running UG & PG EE programs with semiconductor related courses	20

	signed contracts shall be attached as evidence)		between 1 and 3 years including research and innovation outcomes	
			Running only UG EE program with semiconductor related courses including research and innovation outcomes	10
3	**Faculty Experience and Research:** Qualification and Competence of the faculty members –Full Time/Part time/ **(Form B4-I & B4-II).** Relevance of degrees to semiconductor education, tape-out experience	25	Four or more faculty members with relevant degrees to semiconductor field and tape-out experience	25
			Between 2 and 4 faculty members with relevant degrees to semiconductor field and tape-out experience	15
4	**Curriculum Development and Academic Relevance:** UG & PG program and course organization and methodology	30	Integration of foundational and elective courses in UG program. Organization of relevant courses in PG program.	30
5	Accreditation from relevant bodies such as PEC & HEC. Have approved seat allocation from PEC & HEC more than the batch size required from the SERC university, i.e. 40 for MS and 50 for UG.	20	Have valid accreditation of UG & PG programs for two years or more from relevant bodies with allocated number of seats as required.	20
			Have valid accreditation of UG & PG programs for one year or more from PEC & HEC respectively with lesser allocated number of seats as required.	10
6	**Institutional Capacity and Infrastructure Readiness:** Physical & ICT Infrastructure	20	Have adequate infrastructure including dedicated lab space to support the selected UG & MS students	20
7	Industrial linkages and Employability Pathways	10	MoU/Agreement signed with IC Chip Design/Verification companies working in relevant Industry of the project . 02 points for each MoU/Agreement	10
	Project Management & Governance Approach	15	Mechanisms for academic monitoring, curriculum review boards, student performance	15

			tracking, reporting, and committee oversight.	
	Scalability & Sustainability Plan	20	Long-term institutional commitment to sustaining semiconductor programs beyond project funding; future student intake plans, self-sustainability measures, and regional/national outreach.	20
08	Presentation/Demonstration of the Proposed Solution	20	Onsite presentation of proposed solutions by participating bidding public sector universities.	20
	G. Total	**200**		

8.6. Final Ranking and Award Decision

After completion of both technical and the detailed proposal provided under financial evaluations, the proposal with the highest combined score (out of 100%) will be recommended for award, provided it meets all mandatory compliance and legal requirements.

In the event of a tie, preference will be given to the proposal with:

- Better employability of graduated students in the semiconductor technologies.
- Proven project success in public-sector academic environments.

Total Score: 70% Weightage of Technical Score + 30% Weightage of Financial Score

8.7. Instructions for Bidding Public Sector Universities

This document contains all the information pertinent to this solicitation and governs the preparation and submission of Proposals. The technical & financial forms to be filled by Bidding public sector universities for this assignment are annexed with this RFP document. Proposals must be submitted by the deadline, completed on the formats provided by the Executing Agency, with supporting documents, according to the guidelines given in the section titled Instructions & Information for Bidding public sector universities. Proposals will be evaluated by bid evaluation committees constituted by the Executing Agency. Selection of Bidding public sector universities will be on Quality and Cost Based Selection methodology as provided in the Bidding Document.

Proposals must be clearly labeled to indicate the specific lot(s) being addressed. Each lot must be supported by a separate Technical Proposal and a separate Financial Proposal, submitted on E-Pad.

Based on the availability of allocated funds, PSEB reserves the right to determine the exact scope and scale of support to be provided under this RFP for the Semiconductor Education & Research Clusters (SERCs). The implementation process will be guided by strategic priorities, institutional readiness, faculty and infrastructure capacity, and alignment with the national semiconductor development objectives. PSEB may choose to support select universities, training modules, or research facilities from the proposed plans depending on budgetary constraints and technical evaluations. This ensures optimal utilization of resources while maintaining flexibility to address emerging academic and industry needs during project execution.

8.8. Bidding Document

The Bidding public sector universities is expected to examine all instructions, general conditions, forms, terms and specifications contained in the RFP document and its annexures. Failure to comply with instructions will be at the Bidding public sector universities' risk and may affect the evaluation of the Proposal. Proposals that do not comprehensively address the scope of work/ToR and other requirements may be rejected. Inability to comply with applicable instructions, general conditions of contract, terms and specifications may lead to rejection of Proposal.

9. Preparation of Proposal
9.1. Language of the Proposal

Proposals prepared by the Bidding public sector universities and all correspondence and documents relating to the Proposal exchanged between the Bidding public sector universities and the Executing Agency shall be in writing and in English Language.

9.2. Proposal Currency

All prices shall be quoted in Pakistan Rupees (PKR) and all payments will be made in Pakistan Rupees (PKR.).

9.3. Period of Validity of Proposal

Proposals shall remain valid for 180 days from the date of advertisement as provided in the RFP document. In exceptional circumstances, Executing Agency may solicit the Bidding Universities/Institution's consent to an extension of the period of validity without any material changes in the Bidding Document.

9.4. Supporting Documents

While preparing the Technical Proposal, the Bidding public sector universities shall ensure that it provides the Executing Agency with documentary evidence. Bid evaluation committees will evaluate Proposals solely on the basis of documentary evidence submitted in accordance with evaluation criteria described in this Bidding Document.

9.5. Cost of Preparing Proposal

All costs of preparing Proposal and of negotiating with Executing Agency, including visits for discussion with Executing Agency, are not reimbursable.

9.6. Proposal Documents

The Proposal, in binder form, with serial number of each page should comprise the following:

Technical Proposal
Technical Proposal must consist of the following: a)   **Checklist** (Mandatory Documents required with the Proposal) b)   Technical Proposal Submission – Form B1 c)   Bidding public sector universities Profile – Form B2 d)   Relevant Experience of the Bidding public sector universities – Form B3 e)   Qualification, Total Experience and professional Certification/Membership – Form B4-I f)   Composition of Proposed Project Management Team with Organogram – Form B4-II Technical Proposal shall detail the capability and experience of delivering the services specified in the ToR. Bidding public sector universities shall submit details of maximum ten of their most relevant/similar nature assignments for technical evaluation using the prescribed format. Assignments submitted beyond the given number will not be considered. Faculty structure proposed by the Bidding public sector universities for the project (including updated CVs of individuals involved in management and project implementation) in accordance with relevant *Forms*.
Financial Proposal
Financial Proposal must consist of the following: *a)*   Financial Proposal Submission Form

9.7. Format and signing of Proposal

The Proposal shall contain no interlineations, erasures, or overwriting, except, as necessary to correct errors made by the Bidding public sector universities, in which case such corrections shall be initialed by Bidding public sector universities authorized person. The Proposals shall be clear and elaborate. Different parts of Proposals shall be separated using color separators, flags or tags.

Note: *The Technical Proposal must not contain any pricing information whatsoever. Non-compliance will lead to rejection of the Proposal.*

9.8. Submission, Receipt, and Opening of Proposal

Technical and Financial Bids shall be in English language. Single Stage Two Envelop Bidding Procedure of Principal Method of Procurement (i.e. Open Competitive Bidding) will be used by adopting Quality and Cost Based Selection for the subject procurement.

9.8.1. Bids should be submitted electronically ONLY through EPADS. Manual submission of bids is NOT allowed.

9.8.2. For registration and training on EAPDS or in case of any technical difficulty in using EPADS, prospective Bidding public sector universities may contact PPRA Team, Director MIS Room No.109, 1s' Floor, FBC building Sector G-5/2, Islamabad. Contact Number 051-111-137-237.

9.8.3. The bids, prepared in accordance with the instructions in the bidding documents along with bid security instrument (Copy) & Proof of Eligibility documents as specified in bid documents in favor of the undersigned must be submitted through EPADS by 26th September 2025 at 04:00PM. Bids will be opened on the same date at 04:30 PM.

9.8.4. Technical bid mentioned with "Procurement of Services for the Establishment of Semiconductor Education & Research Clusters (SERCs) under the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I", containing technical specifications only (without prices).

9.8.5. Financial proposal shall be mentioned with "Procurement of Services for the Establishment of Semiconductor Education & Research Clusters (SERCs) under the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I" containing the financial proposal.

10. Delivery Timeline

To ensure timely execution and alignment with the objectives of the National Semiconductor Human Resource Development Program (NSHRDP), the selected universities shall execute the program within 60 days after issuance of PO.

10.1. Delivery Period

The PSC approved curriculum will be rolled out and taught to the selected students of 7th & 8th semesters of UG and four (04) semesters of PG programs, as per the academic plan/schedule of the selected university. The standard of the teaching selected curriculum shall be of international level and will be regularly monitored by the procuring agency (PSEB).

10.2. Commencement of Classes

All selected institutions under the SERC component shall be responsible for timely and effective engagements of qualified students in the respective disciplines. This to mention here particularly that the commencement of each semester shall be subject to the approval of designated authority of the procuring agency.

10.2.1. Infrastructure Setup & Readiness

- Complete setup of physical lab spaces (classrooms, labs, EDA workstations, etc.)
- Availability of required internet connectivity, servers, and local/cloud resources for EDA workflows.

10.2.2. Faculty and Human Resource Onboarding

- Deployment of approved faculty, trainers, lab instructors, and technical staff.
- Completion of orientation/training programs (where applicable) prior to the start of academic or training sessions.

10.2.3. Verification and Inspection

- The Project Implementation Unit (PIU) or designated authority will conduct physical and/or virtual inspection(s) to verify that all infrastructure, tools, and required human resources are in place and functional.
- Institutions must cooperate fully with PIU or third-party verifiers during commissioning assessments.

10.2.4. Documentation and Reporting

- Submission of a **Commencement Report** including photographs, signed verification checklists, tool licenses, inventory, faculty/staff deployment, and readiness status.

10.2.5. Curriculum and Training Module Activation

- Finalization and activation of the approved curriculum/training modules.
- Readiness to initiate academic activities immediately after commencement approval.

10.2.6. Commissioning Certificate Issuance

- Upon successful inspection and verification, the PIU shall issue a Commencement Certificate, which will serve as a formal greenlight to begin academic activities and trigger any disbursement milestones.

11. Terms and Conditions

All bidding public sector universities are required to review and comply with the following general and specific terms and conditions of the RFP. These terms shall form the basis of the contractual agreement with the selected SERC partner. PSEB reserves the right to accept or reject any or all proposals, wholly or in part, without assigning any reason or incurring any liability to the bidding universities as per PPRA rules.

12. Force Majeure

- If either party is temporarily rendered unable, wholly or in part by Force Majeure to perform its duties or accept performance by the other party under the Contract it is agreed that on such party, giving notice with full particulars in writing of such Force Majeure to the other party within 14 (fourteen) days after the occurrence of the cause relied on, then the duties, of such party as far as they are affected by such Force Majeure shall be suspended during the continuance of any inability so caused but for no longer period and such cause shall as far as possible be removed with all reasonable speed. Neither party shall be responsible for delay caused by Force Majeure.
- The terms "Force Majeure" as used herein shall mean Acts of God, strikes, lockouts or other industrial disturbance, act of public enemy, war, blockages, insurrections, riots, epidemics (including operational disruptions due to government imposed COVID-19 restrictions), landslides, earthquakes, fires, storms, lightning, flood, washouts, government imposed restrictions due to environmental hazards, civil disturbances, explosion, Governmental Export/Import Restrictions, Government actions/restrictions due to economic and financial hardships, change of priorities and any other causes similar to the kind herein enumerated or of equivalent effect, not within the control of either party and which by the exercise of due care and diligence either party is unable to overcome.
- The terms of this Contract shall be extended for such period of time as may be necessary to complete the work which might have been accomplished but for such suspension. If either party is permanently prevented wholly or in part by Force Majeure for period exceeding 4 (four) months from performing or accepting performance, the party concerned shall have the right to terminate this Contract immediately giving notice with full particulars for such Force Majeure in writing to the other party, and in such event, the other party shall be entitled to compensation for an amount to be fixed by negotiations and mutual agreement.
- If a Force Majeure situation arises, the Bidding public sector universities shall promptly notify PSEB in writing of such conditions and the cause thereof. Unless otherwise directed by PSEB in writing, the Bidding public sector universities shall continue to perform its obligations under the Contract as far as is reasonably practicable and shall seek all reasonable alternative means for performance not prevented by the Force Majeure event.

13. Submission Instructions

Bidding public sector universities must submit their proposals on E-Pad in accordance with the instructions below. Failure to comply with these instructions may result in the rejection of the proposal.

14. Pre-bid meeting

A pre bid meeting will be held on16th September 2025 at 3:00 pm. Participating Institutions are encouraged to join the meeting through the following zoom link:

http://bit.ly/46eYD7Y

15. Submission Address

All proposals must be uploaded on E-Pad to the following address:
https://eprocure.gov.pk/

16. Contact info for Queries

For any technical queries, following contact may please be approached:

Mr. Muhammad Ashraf,
Assist. Director, PSEB
Email: mashraf@pseb.org.pk

For general queries, please contact:

Mr. Muhammad Arif
Manager Administration
Email: rarif@pseb.org.pk, Pakistan Software Export Board, 6th Floor New State life Building, Blue area, Islamabad

PART B

TERMS OF REFERENCE

17. Terms of Reference

The Successful Bidding public sector universities is expected to provide the following services: -

The selected universities under the Semiconductor Education & Research Clusters (SERCs) shall be responsible for the design, development, implementation, and management of comprehensive training and research programs in semiconductor design and related domains. The aim is to equip undergraduate and graduate students with industry-relevant skills, promote indigenous R&D, and establish Pakistan's footprint in the global semiconductor value chain.

17.1. Program Implementation & Delivery

- Develop and deliver revamped undergraduate (BS/BE) and postgraduate (MS/PhD) curricula aligned with international standards in semiconductor education.
- Establish or upgrade labs and teaching infrastructure, ensuring the availability of academic-grade EDA tools, licensed software, servers, and workstations.
- Introduce digital IC design, verification, analog/mixed-signal, and RF domains, with special emphasis on Digital Design & Verification (50–60%).
- Ensure multi-level training delivery (theoretical + practical), incorporating simulation, design flows, verification, and project-based learning.
- Integrate industry advisory inputs to align course content and lab activities with real-world requirements.

17.2. Faculty Development & Knowledge Transfer

- Train faculty members and lab instructors on advanced IC design flows, using academic EDA tools.
- Ensure continuous professional development (CPD) for faculty and trainers through vendor-led workshops, refresher courses, and international certifications.
- Maintain a faculty exchange program (where feasible) with industry professionals and global partner universities.

17.3. Research & Development Promotion

- Establish joint research labs with local industry and R&D organizations in domains such as IC design, embedded systems, and verification.
- Initiate and manage postgraduate research projects targeting indigenous needs (both commercial and defense applications).
- Support participation in international competitions, challenges, and conferences to enhance visibility of Pakistan's talent pool.
- Publish research outcomes in peer-reviewed journals and conferences, strengthening global recognition.

17.4. Industry Engagement & Employability

- Build formal linkages with industry (like MoUs, joint labs, internships, job placement agreements).
- Ensure at least 60% of graduating students are placed in relevant industry positions (local or international) within six (6) months of completion of graduation.
- Facilitate internships and apprenticeships during studies to provide hands-on industry exposure.
- Create career support services, including CV preparation, technical interview training, and soft skills modules.

17.5. Infrastructure & Tools Deployment

- Deploy and maintain a lab with access to servers, storage, and licensed EDA tools.
- Provide secure remote access for students and faculty to ensure continuity of learning and research.
- Ensure scalability of resources to accommodate increasing number of students and projects over the duration of the program.
- Maintain a repository of reusable IP blocks, design flows, and best practices for all participating institutions in the cluster.

17.6. Monitoring, Reporting & Quality Assurance

- Submit quarterly progress reports covering academic delivery, lab utilization, student performance, and industry engagement.
- Provide auditable evidence of trainee numbers, course completions, and job placements.
- Cooperate with third-party monitoring and evaluation teams appointed by PSEB/PIU.
- Implement a continuous feedback mechanism from students, faculty, and industry to refine curriculum and training models.

17.7. Sustainability & Scalability

- Develop a sustainability plan to continue SERC operations beyond initial funding, leveraging revenue models (industry projects, consultancy, alumni networks, etc.).
- Create train-the-trainer programs to ensure that local faculty and staff can independently sustain and expand training capacity.
- Scale the program by onboarding additional universities/partners annually, based on performance and available resources.

PART C

FORMS TO BE SUBMITTED WITH THE PROPOSAL

18. Technical Proposal - Standard Forms

- B1 - Technical Proposal Submission
- B2 - Bidding public sector universities Profile
- B3 - Relevant Experience of the Bidding public sector universities
- B4-I - Qualification, Total Experience and professional Certification/Membership
- B4-II- Composition of Proposed Faculty with Organogram

18.1.   B1. Technical Proposal - Submission Form

To: Project Director
Pakistan Software Export Board
6th Floor New Statelife Building, Bluearea, Islamabad
Islamabad, Pakistan
Tel: +92-51- 111 333 666
Fax: +92-51- 921-9075
Email: NSHRDP@pseb.org.pk
Islamabad, Pakistan

Sir,

We, the undersigned, offer to provide the services for execution of"
***Procurement of Services for Semiconductor Education & Research
Clusters (SERCs) for the Project "National Semiconductor Human
Resource Development Program (NSHRDP) Phase-I"*** in accordance with
your Request for Proposal dated [ADVERTISEMENT DATE]. We are
hereby submitting our Proposal, which includes this Technical Proposal and
Financial   Proposal   on   E-Pads   (https://eprocure.gov.pk/)
(https://eprocure.gov.pk/).

Our Technical Proposal shall be binding upon us subject to the modifications
resulting from Contract negotiations, up to expiration of the validity period
of the Proposal, which is 180 calendar days from the date of advertisement.

We understand you are not bound to accept any Proposal you receive.

Yours sincerely,

Authorized Signature:

Name and Title of Signatory:
Name of Firm: Address:

B2. Bidding public sector universities Profile

Sr. #	Criteria	Response
1	Profile of the Bidding Universities/Institutions: i. Registered age of Bidding Universities/Institutions ii. Names of DEA/HOD/Director/ Partners	
2	i. Location of Bidding public sector universities ii. Number of relevant Faculty Members including their Names & Designations, Contact Numbers & contact numbers	

18.2.   B3. Relevant Experience of the Bidding public sector universities

Experience of Institutes in the relevant to the subject RFP.

Sr, #	Title & Project Synopsis	Name and contact details of Focal Person of the Bidding Universities/Institutions	Bidding Universities/Institutions, Focal Person Name & Phone Numbers	Project Worth	Project Duration
1					
2					
3					
4					

*Please attach relevant documents to corroborate your information.

B4-I. – Qualification, Total Experience and professional Certification/Membership Personnel Summary (Complete for each Team Member)

Name of Faculty:

	Position	
General Information	Name:	Date of Birth:
	Telephone:	
	Fax:	
	Years with Present Employer:	

Employment Record:

Summarize overall professional experience in reverse chronological order.

DD/MM/YY		Bidding public sector universities Specific Tech experience
From	**To**	

Relevant Experience:

Summarize relevant experience in reverse chronological order. Indicate particular technical and managerial experience relevant to the project:

DD/MM/YY		Bidding public sector universities Specific Tech experience
From	To	

Education:

Highest Level of Degree	Relevance of Degree to the Assignment
MPhil	
Masters	
Bachelors	

Certification:

Memberships:

Certification:

I, the undersigned, certify that to the best of my knowledge and belief, these data correctly describe me, my qualifications, and my experience.

_____Date:
[Signature of staff member and authorized representative of the firm] Day/Month/Year

Full name of staff member:

_____

Full name of authorized representative:

_____

18.3.   B4-II – Composition of Proposed Faculty with Organogram

Sr. #	Name/ Designation	Experience/ No. of years	Relevant Experience in Previous Assignments	Proposed Role in this Project

The Bidding public sector universities are encouraged to integrate internationally recognized certifications (e.g., Cadence, Synopsys, Siemens EDA, Mentor Graphics, or equivalent) aligned with the proposed course outlines under the SERC program. These certifications may preferably be offered free of cost (FoC) or at nominal charges to trainees. The procuring agency will conduct a cost–benefit analysis to evaluate the feasibility and added value of such certifications in enhancing employability, industry recognition, and alignment with global standards before making a final decision.

19. Financial Proposal:

The Financial Proposals shall be in the following format:

#	Criterion	What evaluators compare	Unit Cost	GST	Total
1	UG cost per student (annual)	Total PSEB-funded UG cost per student per academic year (tuition/fees claimed from project + teaching allowances claimed + pro-rated OPEX/ overhead attributable to UG)			
2	MS cost per student (annual)	Total PSEB-funded MS cost per student per academic year (tuition/ fees claimed from project + teaching allowances claimed + pro-rated OPEX/ overhead attributable to MS)			
3	Operating expenses & institutional overhead	OPEX + overhead as % of total evaluated financials (after removing fixed/capped items). Lower % = better value			
4	Fee structure clarity & schedule	Transparency of fee heads, per-semester/annual schedule, receipt plan			
5	University cost-sharing / in-kind support	Monetized value of in-kind (labs, space, utilities, licenses, admin support) or fee waivers the university commits			
	Total				

L_1: *Lowest Offered Cost*
L_i: *Offered Cost*