Sno Edge 50™

Preliminary Pinout Definitions

01/27/22

Note: *This document is a preliminary draft only and is subject to change.*

Pin Group Assignments

Notes:

- D and B are non-diff, others are all diff
- PLL is all three PLL pairs, but one is not routed as pair
- xb_pvov indicates numbering seen in OpenXLR8 module

Port Bits	D Nums	xb_pvov	Sno	Sno M2	Sno Edge	Int Bit	GPIO
8	7: 0	[7:0]	D	D	D		S
6	13: 8	[13:8]	B	B	B		S
	: N/A	N/A	ADC	ADC	ADC		
6	19: 14	[19:14]	C	C	C		D
6	27: 22	[25:20]	A	A	A	0	D
6	33: 28	[31:26]	E	E	E	1	D
8	41: 34	[39:32]	G	G	G	2	D
8	49: 42	[47:40]		H	J0	3	D
8	57: 50	[55:48]			J1	3	D
8	65: 58	[63:56]			J2	3	D
8	73: 66	[71:64]			J3	3	D
8	81: 74	[79:72]			K0	4	D
8	89: 82	[87:80]			K1	4	D
8	97: 90	[95:88]			K2	4	D
8	105: 98	[103:96]			K3	4	D
4	109: 106	[107:104]			PL	5	D

Sno Edge 50 Pinout Definitions

This table shows the signals that are connected to the edge connector.
It is arranged to show the front and back side of the board connections side by side

Special Function:	Indicates special functions such as ADC, Clocks or PLLs
FPGA Pin Type	Special function desciptor for FPGA Pad, indicates Diff pair, GND, or VCC
FPGA Pad:	Pad on the FPGA, as seen in the Quartus Pin Planner
FPGA Port Bit:	Port Name and bit in port
FPGA D Bit:	Signal name as seen from Arduino Sketch, based on D pin and/or Port
Edge Pin:	Pin number for the edge connector

Odd Side of Connector						Even Side of Connector					
Special Function	FPGA Pin Type	FPGA PAD	FPGA Port Bit	FPGA D Bit	Edge Pin	Edge Pin	FPGA D Bit	FPGA Port Bit	FPGA PAD	FPGA Pin Type	Special Function
ADC_REF	ADC_REF	E4	ADC_REF	na	1	2				5.0V	
	GND				3	4				USB-	Serial
ADC2in6	L6P	B2	ADC2[6]	na	5	6				USB+	Serial
ADC2in5	L6N	C2	ADC2[5]	na	7	8				GND	
	GND				9	10	na	RESET_N	B10	RESETN	RESET_N
ADC2in7	L8N	B1	ADC2[7]	na	11	12				GND	
ADC2in2	L8P	C1	ADC2[2]	na	13	14	na	ADC2[8]	C3	L2P	ADC2in8
	GND				15	16	na	ADC2[1]	C4	L2N	ADC2in1
ADC1in8	L7P	D1	ADC1[8]	na	17	18				GND	
ADC1in7	L7N	E1	ADC1[7]	na	19	20	na	ADC2[3]	E3	L4N	ADC2in3
	GND				21	22	na	ADC2[4]	F2	L4P	ADC2in4
ADC1in6	L5P	F1	ADC1[6]	na	23	24	na	ADC1[2]	F4	L1P	ADC1in2
ADC1in5	L5N	G2	ADC1[5]	na	25	26	na	ADC1[1]	F5	L1N	ADC1in1
	GND				27	28				GND	
ADC1in4	L3P	G5	ADC1[4]	na	29	30	14	C[0]	J2	L22P	
ADC1in3	L3N	H5	ADC1[3]	na	31	32	15	C[1]	J3	L22N	
	GND				33	34				GND	
	L20P	H6	C[2]	16	35	36	18	C[4]	K2	L29P	
	L20N	J5	C[3]	17	37	38	19	C[5]	L1	L29N	
	GND				39	40				GND	
	Connector Gap									Connector Gap	
	GND				41	42				GND	
	L36N	J6	A[0]	22	43	44	24	A[2]	K5	L41N	
	L36P	K6	A[1]	23	45	46	25	A[3]	L6	L41P	
	GND				47	48				GND	
	L37P	L2	A[4]	26	49	50	na	Clock	L3	FPGA_CLK	CLK
	L37N	M2	A[5]	27	51	52	na	Clock_n	M3	FPGA_CLK	CLK
	GND				53	54				GND	
	B2P	R1	E[0]	28	55	56	30	E[2]	P1	L38P	
	B2N	P2	E[1]	29	57	58	31	E[3]	N2	L38N	
	GND				59	60				GND	
	B6P	T2	E[4]	32	61	62	34	G[0]	R2	B4P	
	B6N	T3	E[5]	33	63	64	35	G[1]	R3	B4N	
	GND				65	66				GND	
PLL	L59N	N3	PL[0]	104	67	68	36	G[2]	R4	B5N	
PLL	L59P	N4	PL[1]	105	69	70	37	G[3]	P5	B5P	
	GND				71	72				GND	
	B1N	P4	G[4]	38	73	74	40	G[6]	T4	B14P	
	B1P	N5	G[5]	39	75	76	41	G[7]	T5	B14N	
	GND				77	78				GND	
no diff pair	B13P	R5	D[0]	0	79	80	1	D[1]	R6	B13N	no diff pair
	3.3V				81	82				3.3V	
	B16P	P6	J[0]	42	83	84	44	J[2]	R8	B17P	
	B16N	R7	J[1]	43	85	86	45	J[3]	T8	B17N	
	3.3V				87	88				3.3V	
no diff pair	B15P	L8	D[2]	2	89	90	3	D[3]	M7	B15N	no diff pair
	B3N	M6	J[4]	46	91	92	48	J[6]	M8	B20N	
	B3P	L7	J[5]	47	93	94	49	J[7]	M9	B20P	
	3.3V				95	96				3.3V	
no diff pair	B18P	P8	D[4]	4	97	98	5	D[5]	P9	B18N	no diff pair
	B36P	L9	J[8]	50	99	100	52	J[10]	R9	B19P	
	B36N	M10	J[9]	51	101	102	53	J[11]	T9	B19N	
	3.3V				103	104				3.3V	
	B22P	R10	J[12]	54	105	106	56	J[14]	P10	B34N	
	B22N	T11	J[13]	55	107	108	57	J[15]	P11	B34P	
SDA	B57N	M11	SDA	na	109	110	na	SCL	L10	B57P	SCL
	3.3V				111	112				3.3V	
	B35N	R11	J[16]	58	113	114	60	J[18]	P12	B37P	
	B35P	R12	J[17]	59	115	116	61	J[19]	P13	B37N	
	3.3V				117	118				3.3V	
	R2P	T14	D[6]	6	119	120	7	D[7]	T15	R2N	no diff pair
	GND				121	122				GND	
	R1N	R14	J[20]	62	123	124	64	J[22]	N14	R27P	
	R1P	P14	J[21]	63	125	126	65	J[23]	P15	R27N	
	GND				127	128				GND	
	R29N	P16	J[24]	66	129	130	8	B[0]	L12	R25N	no diff pair
	R29P	N16	J[25]	67	131	132				GND	
	GND				133	134	68	J[26]	M14	R28N	
	R33P	M16	J[28]	70	135	136	69	J[27]	M15	R28P	
	R33N	L16	J[29]	71	137	138				GND	
	GND				139	140	72	J[30]	K14	R32P	
	R30P	K11	K[0]	74	141	142	73	J[31]	L15	R32N	
	R30N	K12	K[1]	75	143	144				GND	
	GND				145	146	76	K[2]	J11	R38P	
no diff pair	R39N	K15	B[1]	9	147	148	77	K[3]	J12	R38N	
	GND				149	150				GND	
	R40P	J15	K[4]	78	151	152	80	K[6]	H15	R41P	
	R40N	J16	K[5]	79	153	154	81	K[7]	H16	R41N	
	GND				155	156				GND	
	R44P	H11	K[8]	82	157	158	84	K[10]	G11	R50P	
	R44N	H12	K[9]	83	159	160	85	K[11]	G12	R50N	
	GND				161	162				GND	
pair w/170	R46N	G15	B[2]	10	163	164	86	K[12]	G16	R47P	
	GND				165	166	87	K[13]	F16	R47N	
	R51P	F14	K[14]	88	167	168				GND	
	R51N	E14	K[15]	89	169	170	11	B[3]	G14	R46P	pair w/163
	GND				171	172				GND	
	R52P	E15	K[16]	90	173	174	108	PL[2]	D14	R69P	PLL
	R52N	E16	K[17]	91	175	176	109	PL[3]	C14	R69N	PLL
	GND				177	178				GND	
	R42P	D16	K[18]	92	179	180	94	K[20]	D15	R70P	
	R42N	C16	K[19]	93	181	182	95	K[21]	C15	R70N	
	GND				183	184				GND	
no diff pair	T17N	F12	B[4]	12	185	186	96	K[22]	C13	T2P	
	GND				187	188	97	K[23]	C12	T2N	
	T30P	B13	K[24]	98	189	190				GND	
	T30N	A13	K[25]	99	191	192	100	K[26]	D12	T1P	
	GND				193	194	101	K[27]	E11	T1N	
	T28P	F10	K[28]	102	195	196				GND	
	T28N	E10	K[29]	103	197	198	104	K[30]	B12	T41P	
no diff pair	T43P	A11	B[5]	13	199	200	105	K[31]	B11	T41N	